PACKAGE SUBSTRATE AND PROCESS THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 92122340, filed on August 14, 2003.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a chip package and process thereof; more particularly, the present invention relates to a package substrate and process thereof for a wire bonding type package.

Description of the Related Art

[0002] Because of the evolution of the semiconductor technology and the market requirement, the semiconductor industry has developed high integrated and high speed electronic devices. For the semiconductor package technology, for example, chip package technology, the manufacturing of chip carriers and the assembly of the passive components are all very important in the semiconductor industry.

[0003] For the chip package technology, a die generated from performing semiconductor manufacturing processes over a wafer and by cutting the wafer, is assembled on a surface of a carrier by, for example, a wire bonding technology or a flip chip bonding technology, wherein the carrier is, for example, a leadframe or a substrate. The die has many die pads; therefore, the die can be electrically connected to the external electronic devices by connecting the die pads of the die to the transmission

circuits and contacts of the carrier. In addition, after the die pads of the die are electrically connected to the contacts of the carrier by a wire bonding technology, a dielectric material can cover the die and conductive wires for protecting the die and the conductive wires. Therefore, a manufacturing process of chip package is complete and a chip package is formed thereby.

[0004] FIGS. 1A~1C are a schematic process flow illustrating a conventional manufacturing process of a wire bonding type package with a passive component. Please referring to FIG. 1A, a carrier 110 is provided, which has a die bonding area 112, and at least a power pad 116, a ground pad 114 and a signal pad 118 are disposed on the surface of the carrier 110 outside the die bonding area 112. In addition, the signal pad 118 is disposed farther from the die bonding area 112 than the power pad 116 and the ground pad 114. The power pad 116, the ground pad 114 and the signal pad 118 are formed, for example, by a patterned conductive layer, and the surface of the patterned conductive layer can be covered with a patterned solder mask layer 140. The solder mask layer 140 has a plurality of openings 142 which expose the surfaces of the power pad 116, the ground pad 114 and the signal pad 118 respectively. In addition, in order to prevent the oxidation of pads 114, 116 and 118, a metal layer 144 is formed on the exposed surfaces of the power pad 116, the ground pad 114 and the signal pad 118. The material of the metal layer 244 can be, for example, nickel, gold or alloy thereof. Therefore, the reliability of a subsequent wire bonding process can be improved.

[0005] Referring to FIG. 1B, a die 120 is disposed on the surface of the carrier 110, and bonded on the die bonding area 112 with the backside 122 of the die 120. The active surface 124 of the die 120 has a plurality of die pads 126

[0006] Referring to FIG. 1C, two ends of each conductive wire 134, 136 and 138 are connected to one of the die pads 126 of the die 120 and to the power pad 116, the ground pad 114 and the signal pad 118, respectively. In addition, in order to improve the electrical performance of the chip package 100, a small passive component 130 is usually used to be bonded on the surface of the carrier 110 by surface mount technology (SMT) for reducing signal noise crosstalk and maintaining signal transmission quality. The passive component 130 can be, for example, an inductor or a capacitor. The passive component 130 is disposed between the power pad 116 and the ground pad 114 of the carrier 110, and two electrodes 132a and 132b of the passive component 130 are soldered to the power pad 116 and the ground pad 114, respectively.

[0007] Referring to FIG. 1C, it should be noted that the passive component 130 is disposed, for example, under the signal conductive wire 138, and the signal conductive wire 138 is over the passive component 130 and does not touch the electrode 132a. However, the conductive wire 136 connected to the die pad 126 and the power pad 116 must be over the passive component 130, and is then bonded to the surface of the power pad 116. Because the conductive wire 136 must be an arc for crossing over the passive component 136, the length of the conductive wire 136 increases, so the length of signal transmission path increases. Therefore, the electrical performance of the die 120 becomes worse and the layout space of neighboring conductive wires is affected.

SUMMARY OF THE INVENTION

[0008] Accordingly, one object of the present invention provides a manufacturing process of package substrate in order to improve yield and reliability of a subsequent wire bonding process.

[0009] In order to achieve the object of the present invention mentioned above, the present invention discloses a manufacturing process of package substrate comprising providing a carrier, a surface of the carrier having a die bonding area; forming a patterned conductive layer on the surface of the carrier, wherein the patterned conductive layer at least comprises a power pad, a ground pad and a signal pad; then disposing at least one passive component between the power pad and the ground pad, the passive component having at least two electrodes which are separately electrically connected to the power pad and the ground pad; and finally forming a metal layer on surfaces of the electrodes and exposed surfaces of the power pad, the ground pad and the signal pad.

[0010] In order to make the aforementioned and other objects, features and advantages of the present invention understandable, a preferred embodiment accompanying figures is described in detail as follow.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIGS. 1A~1C are a schematic illustrating the progression of a conventional manufacturing process of a wire bonding type package.

[0012] FIGS. 2A~2C are a schematic illustrating the progression of a manufacturing process of a wire bonding type package in accordance with the present invention.

DESCRIPTION OF SOME EMBODIMENTS

[0013] FIGS. 2A~2C are a schematic illustrating the progression of a manufacturing process of a wire bonding package in accordance with an embodiment of the present invention. Referring to FIG. 2A, a carrier 210 is provided. The carrier 210 can be, for example, a substrate which has a surface having a die bonding area 212, and a plurality of bonding pads including at least a power pad 216, a ground pad 214 and a signal pad 218 are disposed on the surface of the carrier 210. In addition, the power pad 216 and the ground pad 214 are disposed outside the die bonding area 212, and are formed, for example, by portions of the power ring (not shown) and a ground ring (not shown) around the die bonding area 212, respectively. The signal pad 218 is farther from the die bonding area 212 than the power pad 216 and the ground pad 214. The power pad 216, the ground pad 214 and the signal pad 218 are formed, for example, by a patterned conductive layer, and the surface of the patterned conductive layer can be covered with a patterned solder mask layer 240. The solder mask layer 240 has a plurality of openings 242 which expose the surfaces of the power pad 216, the ground pad 214 and the signal pad 218, respectively.

[0014] Referring to FIG. 2A, in the preferred embodiment, a passive component 230 is disposed between the power pad 216 and the ground pad 214. The passive component 230 has at least two electrodes 232a and 232b which can be bonded on the surfaces of the power pad 216 and the ground pad 214 by surface mount technology (SMT) for reducing signal noise crosstalk and maintaining quality of signal transmission. The passive component 230 can be, for example, an inductor or a capacitor, and the material of the electrodes 232a and 232b can be, for example, Sn-Pb alloy.

[0015] Next, referring to FIG. 2B, a metal layer 244 is formed on the surfaces of the electrodes 232a and 232b, and exposed surfaces of the power pad 216, the ground pad 214 and the signal pad 218 for avoiding oxidation of the contacts 214, 216 and 218. The material of the metal layer 244 can be, for example, nickel, gold or alloy thereof, which can be formed by an electroplating method. In addition, the material of the metal layer 244 has a good wire bonding property with a gold wire for improving the reliability of the subsequent wire bonding process.

[0016] Referring to FIG. 2C, a die 220 is disposed on the surface of the carrier 210, and bonded on the die bonding area 212 with the backside 222 of the die 220. The active surface 224 of the die 220 has a plurality of die pads 226 which are respectively corresponding to the power pad 216, the ground pad 214 and the signal pad 218.

[0017] Referring to FIG. 2C, in order to reduce the length of the first conductive wires 236a and 236b, at least one end of the first conductive wire 236a is connected to the electrode 232a of the passive component 230, wherein the two ends of the first conductive wire 236a are connected to the die pad 226a of the die 220 and the electrode 232a of the passive component 230. The two ends of another first conductive wire 236b are connected to the die pad 226b of the die 220 and the electrode 232b of the passive component 230. Because the first conductive wire 236a does not cross over the passive component 230, but directly be bonded to the electrode 232a of the passive component 230, the length of the first conductive wire 236a is reduced, and the path of signals going through the first conductive wire 236a can be shortened. Therefore, the electrical performance of the die 220 is improved and the layout spaces of neighboring conductive wires are increased. In addition, two ends of the second conductive wire 238 can be connected to the die pad 236c of the die 220 and the signal pad 218 of the carrier 210,

respectively. The second conductive wire 238 can cross over the passive component 230 thereby not touching the electrodes 232a and 232b of the passive component 230.

[0018] From the above descriptions, the manufacturing process of package substrate of the present invention is firstly disposing at least one passive component between the power pad and the ground pad of the carrier, wherein two electrodes of the passive component connecting to the power pad and the ground pad, respectively; and then forming a metal layer on the electrodes of the passive component and exposed surfaces of the power pad, the ground pad and the signal pad.

[0019] The manufacturing process of package substrate of the present invention has at least following advantages:

(1) A metal layer is formed on the electrode surfaces of the passive component and exposed surfaces of the power pad, the ground pad and the signal pad by performing an electroplating step. An end of the conductive wire is directly connected to an electrode of the passive component. Thus, the yield and reliability of chip package can be effectively improved.

(2) An end of the conductive wire is directly connected to an electrode of the passive component; therefore, the length of the conductive wire is reduced, and the signal transmission path going through the conductive wire is shortened. Accordingly, the electrical performance of the chip package is improved and the layout spaces of neighboring conductive wires are increased.

[0020] Although the present invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be constructed broadly to include other variants and embodiments of the invention which

may be made by those skilled in the field of this art without departing from the scope and range of equivalents of the invention.